

PTO/SB/08a/b (08-03)



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


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<b>Substitute for form 1449A/B/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				<b>Complete If Known</b>	
				Application Number	10/779,557
				Filing Date	February 6, 2004
				First Named Inventor	Franz Hofmann
				Art Unit	<del>11A</del> 2822
				Examiner Name	<del>Not Yet Assigned</del> Soward
Sheet	1	of	1	Attorney Docket Number	20046/0200847-USO

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	AA	US-6,335,554-B1	01-01-2002	Yoshikawa	
	AB	US-6,388,293-B1	05-14-2002	Ogura et al.	

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Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
		Country Code <sup>4</sup> -Number <sup>5</sup> -Kind Code <sup>6</sup> (if known)	MM-DD-YYYY			
	BA	DE-100 36 911-A1	02-14-2002	Hofmann, Franz et al.		X
	BB	JP-2001 156188-A1	06-08-2001	Yoshikawa Kuniyoshi		X

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T <sup>2</sup>
	CA	Hayashi Y et al.: "Twin Monos Cell With Dual Control Gates"; 2000 Symposium on VLSI TECHNOLOGY, Digest of Technical Papers, Honolulu, HI, June 13-15, 2000, Symposium on VLSI Technology, New York, NY; IEEE, US, 13 June 2000, pages 122-123, XP000970787.			
	CB	PATENT ABSTRACTS OF JAPAN, vol. 2000, no. 22, 9 March 2001 & JP 2001 148434 A (New Heiro: KK; Halo LSI Design & Device Technol Inc), 29 May 2001, abstract.			
	CC	Naruke K et al: "A New Flash-Erase EEPROM Cell with a Sidewall Select-Gate on Its Source Side"; Tech. Digest, 1989, IEDM 89-603, pages 25.7.1 - 25.7.4.			

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Examiner Signature		Date Considered	5-19-05
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